IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of fabricating a submicron semiconductor device comprising:

forming an oxide layer on a substrate;

forming a polysilicon layer on said oxide layer;

forming a hard mask on said polysilicon layer;

depositing a photoresist on said hard mask and patterning said photoresist by using a mask;

etching said hard mask by plasma etching to form a thin hard mask pattern by using the photoresist pattern as an etching mask so that the hard mask pattern can have a narrower width than that of the photoresist pattern; [[and]]

etching said polysilicon layer by using the hard mask pattern as an etching mask[[,]] to form a gate electrode in said polysilicon layer having a desired critical dimension smaller than a corresponding critical dimension in said hard mask; and

etching a polymer formed as a residual product resulting from etching said polysilicon layer,

wherein said hard mask is a SiH_4 oxide deposited by means of PE-CVD.

2. (Original) The method according to claim 1, further comprising depositing an ARC on said hard mask so as to lower reflectivity.

3. (Original) The method according to claim 2, wherein said ARC is of organic or inorganic material.

4. (Original) The method according to claim 1, wherein said photoresist patterning is performed using a KrF laser as a light source.

5. (Canceled)

6. (Currently Amended) A method of fabricating a submicron semiconductor device comprising:

forming an oxide layer on a substrate;

forming a polysilicon layer on said oxide layer;

forming a hard mask on said polysilicon layer;

depositing a photoresist on said hard mask and patterning said photoresist by using a mask;

etching said hard mask by plasma etching to form a thin hard mask pattern by using the photoresist pattern as an etching mask so that the hard mask pattern can have a narrower width than that of the photoresist pattern; [[and]]

etching said polysilicon layer by using the hard mask pattern as an etching mask, to form a gate electrode in said polysilicon layer having a desired critical dimension smaller than a corresponding critical dimension in said hard mask; and

etching a polymer formed as a residual product resulting from etching said polysilicon layer,

wherein said hard mask has a thickness of about 150~400Å.

7. (Canceled)

8. (Previously presented) The method according to claim 1, wherein said hard mask is etched by means of isotropic etching.

9. (Original) The method according to claim 8, wherein said isotropic etching is plasma etching.

10. (Original) The method according to claim 9, wherein said plasma etching uses SF_6 gas as an etching gas.

11. (Original) The method according to claim 1, wherein said etching is performed through plasma etching.

12. (Original) The method according to claim 11, wherein said plasma etching is performed using Cl_2/HBr, Cl_2/O_2 or HBr/O_2 as an etching gas so that the selectivity of said polysilicon to said oxide can be about 10 to 1.

13. (Currently Amended) A method of fabricating a submicron semiconductor device comprising:

forming an oxide layer on a substrate;

forming a polysilicon layer on said oxide layer;

forming a hard mask on said polysilicon layer;

depositing a photoresist on said hard mask and patterning said photoresist by using a mask;

etching said hard mask by plasma etching to form a thin hard mask pattern by using the photoresist pattern as an etching mask so that the hard mask pattern can have a narrower width than that of the photoresist pattern;

etching said polysilicon layer by using the hard mask pattern as an etching mask;

etching a polymer formed as a residual product resulting from etching said polysilicon layer; and

selectively removing said hard mask pattern using a wet etch while protecting said polysilicon layer and said oxide layer from etching.

14. (Original) The method according to claim 13, further comprising depositing an ARC on said hard mask so as to lower reflectivity.

15. (Original) The method according to claim 13, wherein said removing of hard mask is performed through wet etching by HF gas, which is generated gasifying a solution of about 39% HF, at the same time that said gas protects a polysilicon gate and a gate oxide.

16. (Original) The method according to claim 15, wherein said HF gas is formed through spraying N_2 gas onto the surface of a chemical bath containing HF solution.

17. (Original) The method according to claim 13, wherein said wet-etching is performed on a hot plate having a temperature of about 50~90°C.

18. (Original) The method according to claim 13, wherein an etching rate of said wet-etching is less than about 1Å/min for said gate oxide and more than about 200Å/min for said hard mask.

19. (Original) The method according to claim 13, wherein said photoresist patterning is performed using a KrF Laser as a light source.

20. (New) The method according to claim 1, wherein said polymer is etched by using a dilute HF cleaning process.

21. (New) The method according to claim 6, wherein said polymer is etched by using a dilute HF cleaning process.

22. (New) The method according to claim 13, wherein said polymer is etched by using a dilute HF cleaning process.